UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/835,170	04/13/2001	Spencer Gold	P5213/SMQ-041	4882

959 7590 05/17/2005

LAHIVE & COCKFIELD, LLP.
28 STATE STREET
BOSTON, MA 02109

EXAMINER	
CHAUDRY, MUJTABA M	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 05/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/835,170	GOLD, SPENCER	
	Examiner	Art Unit	
	Mujtaba K. Chaudry	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 24-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 24-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Applicant's arguments/amendments with respect to amended claims 1 and 24 and original claims 2-6 and 25-29 filed March 17, 2005 have been fully considered but are not persuasive. The Examiner would like to point out that this action is made final (See MPEP 706.07a).

Applicant contends, "...Yamada (prior art of record) fails to disclose an integrated circuit..." The Examiner would like to point out that Yamada teaches (Figure 5) a block diagram showing an example of circuit configuration of the in which both the address scramble function and the wrap address conversion function for the SDRAM are included. Yamada teaches that when both of the address inversion scramble function and the wrap conversion operation for testing the SDRAM are to be used, the present invention can be configured as shown in FIG. 5. In this example, the internal logic structure of the Y scramble memory 32 is formed of a combination of the logic circuit information for the sequential address mode of FIG. 3 and the logic circuit information for the scramble conversion. Further, the internal logic structure of the Y scramble memory 32 can be formed of a combination of the logic circuit information for the interleave address mode of FIG. 4 and the logic circuit information for the scramble conversion. In this case, however, a signal for separating the wrap conversion circuit from the scramble circuit cannot be taken out, and thus, a signal for failure analysis cannot be obtained. In the above embodiment, the wrap conversion function is performed in the Y scramble memory. However, it is also possible to include the wrap conversion function in the X scramble memory

as well. The Examiner would like to point out that Yamada does not teach that all the elements are not on a integrated circuit and one of ordinary skill in the art would have recognized that testing an SRAM would high likely be done on a integrated circuit or a semiconductor device as stated in the present application. Furthermore, the Examiner would like to point out that the even if all the elements were not to be on the same circuit, the claims of the present application would not be patentably distinct over Yamada. See ***In re Larson 144 USPQ 347 (CCPA 1965)***.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies are not recited in the rejected claim(s). For example, Applicant contends, "Yamada (prior art of record) fails to teach a test generator having memory storage device." Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

The Examiner disagrees with the Applicant and maintains rejections with respect to amended claims 1 and 24 and original claims 2-6 and 25-29. All arguments have been considered. It is the Examiner's conclusion that amended claims 1 and 24 and original claims 2-6 and 25-29, as presented, are not patentably distinct or non-obvious over the prior art of record. See prior office action:

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 and 24 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamada et al. (USPN 5854801). Prior office action:

As per claims 1 and 24, Yamada et al. (herein after: Yamada) teaches (title, abstract and Figure 1) a method and apparatus for generating patterns for SDRAM memory. A test pattern is generated for the SDRAM by having a specific wrap conversion circuit or an address conversion method. The wrap conversion circuit is provided to receive two kinds of data from a pattern generator and converts the data through a predetermined logic circuit information. The test pattern generation method for the SDRAM is carried out by inputting the column address data Y0-Y2 and the wrap address data Z0-Z2, and by generating output data which has been converted by a predetermined logic equation. The test pattern generation apparatus and method can also include an address inversion scramble for the converted output. Furthermore, Yamada teaches (Figure 1) the wrap address conversion circuit 40 is provided at an output of a pattern generator 10. For the wrap address conversion circuit 40, data (Y0-Y8) corresponding to the bit length of the column address of the SDRAM is provided from the pattern generator 10. At the same time, data (Z0-Z2) corresponding to the bit length of the wrap address of the SDRAM is provided to the wrap address conversion circuit 40 from the pattern generator 10. Yamada also teaches (col. 4, lines 25-65) the address inversion scramble is used for converting the address

between the logical address and the physical address of the device under test. This is a function to convert the address because the chip alignment within the device to be tested is freely designed and determined to meet the physical and operational conditions of the device for each kind of devices and such an alignment does not match the logical address given at the outside of the device. Thus, the address inversion scramble is a function necessary to perform failure analysis with respect to the internal operation of the device under test.

Claim Rejections - 35 USC § 103

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 2-6 and 25-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada et al. (USPN 5854801).

As per claims 2-4 and 25-27, Yamada et al. (herein after: Yamada) substantially teaches, in view of above rejections, a conversion circuit as shown in Figure 1.

Yamada does not explicitly teach the conversion circuit to comprise of a ROM, RAM or EEPROM as stated in the present application.

However, Yamada teaches (col. 2, lines 10-63) a test pattern generation apparatus is provided to effectively test an SDRAM. The pattern generation apparatus includes a-wrap

address conversion means which is provided with two (2) kinds of data (Y0-Y2) and (Z0-Z2) from a pattern generator and outputs converted addresses which have been converted based on a predetermined logic circuit information in the conversion means. The Examiner would like to point out that the conversion circuit inherently has to have temporarily storage device, for example a RAM, which is a type of storage memory that can be used while operating. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate a RAM, ROM or EEPROM within the conversion circuit of Yamada. This modification would have been obvious to one of ordinary skill because one of ordinary skill would have recognized that the use of EEPROM, RAM or ROM allows the electronic device to detect nonfunctional memory cell locations.

As per claims 5-6 and 28-29, Yamada et al. (herein after: Yamada) substantially teaches, in view of above rejections, the address inversion scramble is used for converting the address between the logical address and the physical address of the device under test. This is a function to convert the address because the chip alignment within the device to be tested is freely designed and determined to meet the physical and operational conditions of the device for each kind of devices and such an alignment does not match the logical address given at the outside of the device. Thus, the address inversion scramble is a function necessary to perform failure analysis with respect to the internal operation of the device under test. Further, the output of the wrap conversion circuit 40 can be given to a failure analysis apparatus.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiries concerning this communication should be directed to the examiner, Mujtaba Chaudry who may be reached at 571-272-3817. The examiner may normally be reached Mon – Thur 6:30 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, please contact the examiner's supervisor, Albert DeCady at 571-272-3819.

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Mujtaba Chaudry
Art Unit 2133
May 3, 2005